Amendments to the Specification:

[0014] In another embodiment of invention as shown in Fig. 4A, the time at which oscillator 42 is disabled is determined from drive signal 502, based on the amplitude and width of positive pulses applied to transistor 500 (see Fig. 2). In this manner oscillator 42 is disabled before predetermined time $t = t_3$ very soon after controller 602 commences operating and generating drive signal 502, which may be in the form of short pulses. One possible circuit implementation is shown in Fig. 4A, where additional circuit 509, comprising diode 503, resistor 504, capacitor 505 and resistor 506, receives voltage pulses 502 from the gate of transistor 500. The voltage on capacitor 505 depends on the amplitude and duration of voltage pulses 502, the capacitance of capacitor 505, and resistance of resistors 504 and 506. The voltage on capacitor ~~506~~ 505 is compared with reference voltage V_R in comparator 507 and, when the voltage on capacitor ~~506~~ 505 exceeds reference voltage V_R, comparator 507 generates logic low signal 510 on its output which is fed into protection and control circuit 41 and oscillator 42 becomes disabled. Note that even when the circuit of Fig. 4A is used, it is advantageous to disable oscillator 42 after predetermined time $t = t_3$ if controller 602, and consequently the converter, is not operating or the voltage on winding N3 (Fig. 2) is not big enough to provide bias voltage V_{ccs}. Such conditions could be, for example, if over-current protection is activated, in which case the converter may operate with a very small duty cycle and consequently very narrow voltage pulses 502 will not trip comparator 507 (Fig. 4A) and narrow pulses on winding N_3 (Fig.2) will not be enough to provide the minimum voltage on capacitor 60 needed for operation of controller 602.